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November 21, 2008

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Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

Art Unit 2416

Attn: Mail Stop Appeal Brief -- Patents

Re: U.S. Utility Patent Application  
Application No. 09/909,896; Filing or 371(c) Date: July 23, 2001  
For: **Methods and Systems for Digitally Processing Optical Data Signals**  
Inventors: AGAZZI *et al.*  
Our Ref: 1875.1100001

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Brief on Appeal Under 37 C.F.R. §41.37;
2. Fee transmittal;
3. Credit Card Payment Form (PTO-2038) in the amount of \$540.00 to cover:

\$540 for filing a brief in support of an appeal; and

4. Return postcard.

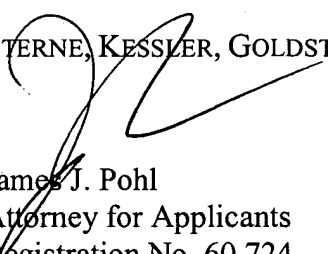
It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Commissioner for Patents  
November 21, 2008  
Page 2

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

  
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

James J. Pohl  
Attorney for Applicants  
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JTH/JJP/la  
Enclosure(s)

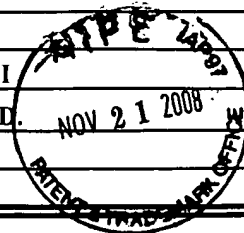
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**FEE TRANSMITTAL**  
**For FY 2009**☐ Applicant claims small entity status. See 37 CFR 1.27**TOTAL AMOUNT OF PAYMENT** (\$) **540****Complete if Known**

Application Number	09/909,896
Filing Date	July 23, 2001
First Named Inventor	Oscar AGAZZI
Examiner Name	Nguyen, Toan D.
Art Unit	2416
Attorney Docket No.	1875.1100001

**METHOD OF PAYMENT** (check all that apply)
☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): \_\_\_\_\_

☒ Deposit Account Deposit Account Number: **19-0036** Deposit Account Name: **Sterne, Kessler, Goldstein & Fox P.L.L.C.**

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

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☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

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**FEE CALCULATION****1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	330	165	540	270	220	110	
Design	220	110	100	50	140	70	
Plant	220	110	330	165	170	85	
Reissue	330	165	540	270	650	325	
Provisional	220	110	0	0	0	0	

**2. EXCESS CLAIM FEES**

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	52	26
Each independent claim over 3 (including Reissues)	220	110
Multiple dependent claims	390	195

<b>Total Claims</b>	<b>Extra Claims</b>	<b>Fee (\$)</b>	<b>Fee Paid (\$)</b>	<b>Multiple Dependent Claims</b>
- 20 or HP =	x	=		<b>Fee (\$)</b>

HP = highest number of total claims paid for, if greater than 20.

<b>Indep. Claims</b>	<b>Extra Claims</b>	<b>Fee (\$)</b>	<b>Fee Paid (\$)</b>
- 3 or HP =	x	=	

HP = highest number of independent claims paid for, if greater than 3.

**3. APPLICATION SIZE FEE**

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

<b>Total Sheets</b>	<b>Extra Sheets</b>	<b>Number of each additional 50 or fraction thereof</b>	<b>Fee (\$)</b>	<b>Fee Paid (\$)</b>
- 100 =	/ 50 =	(round up to a whole number) x	=	

**4. OTHER FEE(S)**

Non-English Specification, \$130 fee (no small entity discount)

Other (e.g., late filing surcharge): **Filing a brief in support of an appeal****Fees Paid (\$)****540****SUBMITTED BY**

Signature	Registration No. (Attorney/Agent)	Telephone
Name (Print/Type)		Date

**James J. Poff****60,724****(202) 371-2600****11/21/08**

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

AGAZZI *et al.*

Appl. No.: 09/909,896

Filed: July 23, 2001

For: **Methods and Systems for Digitally  
Processing Optical Data Signals**

Confirmation No.: 9207

Art Unit: 2416

Examiner: Nguyen, Toan D.

Atty. Docket: 1875.1100001

**Brief on Appeal Under 37 C.F.R. § 41.37**

***Mail Stop Appeal Brief - Patents***

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

A Notice of Appeal from the final rejections of claims 1-52, 54, and 56 was filed on July 9, 2008. Appellants hereby file one copy of this Appeal Brief, together with the required fee set forth in 37 C.F.R. § 41.20(b)(2).

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

11/24/2008 JADD01 00000011 09909896

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***I. Real Party In Interest (37 C.F.R. § 41.37(c)(1)(i))***

The real party in interest in this appeal is Broadcom Corporation, having its principal place of business at 5300 California Avenue, Irvine, California 92617. An assignment of all right, title and interest in and to the above-captioned patent application from inventors Oscar Agazzi and Venu Gopinathan to Broadcom Corporation was recorded in the U.S. Patent & Trademark Office (USPTO) on July 23, 2001 at Reel 012016, Frame 0161.

***II. Related Appeals and Interferences (37 C.F.R. § 41.37(c)(1)(ii))***

The Appellants, including the undersigned legal representative and the assignee of the above-captioned application, are aware of no pending appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board of Patent Appeals and Interferences ("the Board") in the pending appeal.

***III. Status of Claims (37 C.F.R. § 41.37(c)(1)(iii))***

The Application was filed on July 23, 2001 and was assigned U.S. Application No. 09/909,896 ("the '896 application"). The '896 application originally included claims 1-51. The Examiner mailed a Non-final Office Action rejecting claims 1-51 on January 4, 2005. In an Amendment and Reply filed July 1, 2005, the Appellants amended claims 1-51. The Appellants also presented arguments against the rejections. A Final Office Action rejecting claims 1-51 was mailed August 30, 2005. In an After-final Amendment and Reply filed October 25, 2005, the Appellants amended claims 1-2, 8-9, and 18. The Appellants also presented arguments against the rejections. An Advisory Action was mailed November 17, 2005, in which the Examiner upheld the final rejection of claims 1-51. On November 30, 2005, the Appellants filed a Request for Continued Examination.

The Examiner mailed a Non-final Office Action rejecting claims 1-51 on February 8, 2006. In a Reply filed May 8, 2006, the Appellants presented arguments against the rejections. A Non-final Office Action rejecting claims 1-51 was mailed July 24, 2006. In an Amendment and Reply filed October 23, 2006, the Appellants amended claims 1, 9, and 18. New claims 52-57 were added. The Appellants also presented arguments against the rejections. A Final Office Action rejecting claims 1-57 was mailed January 5, 2007. In an After-final Amendment and Reply and a Request for Continued Examination filed July 5, 2007, the Appellants amended claims 1, 9, and 18. Claims 53, 55, and 57 were cancelled. The Appellants also presented arguments against the rejections.

The Examiner mailed a Non-final Office Action rejecting claims 1-52, 54, and 56 on September 21, 2007. In a Reply filed January 22, 2008, the Appellants presented



arguments against the rejections (herein "previous Reply"). A Final Office Action rejecting claims 1-52, 54, and 56 was mailed April 9, 2008. Claims 1-52, 54, and 56 are on appeal. A copy of the claims on appeal can be found in the attached Claims Appendix.

***IV. Status of Amendments (37 C.F.R. § 41.37(c)(1)(iv))***

No amendments to the claims have been submitted subsequent to the Final Office Action dated April 9, 2008. All amendments to the claims previously presented during prosecution have been entered.

***V. Summary of Claimed Subject Matter (37 C.F.R. § 41.37(c)(1)(v))***

A concise explanation of the invention is provided below for each of the independent claims involved in the appeal. The following explanation refers to the specification by page and line number, and to the drawings, if any, by reference characters.

Independent claim 1 recites a method of receiving an optical data signal. The method includes steps of:

(1) receiving an optical data signal (Specification p. 3, lns. 3-6; p. 11, ln. 17 to p. 13, ln. 28; p. 21, lns. 8-15; p. 37, lns. 2-6; paras. [0008], [0065]-[0073], and [0119]; originally-filed claim 1; element 102 in FIG. 1C; element 112 in FIGS. 1B and 9; element 114 in FIGS. 1B-C and 11A; and elements 903-1 to 903-4 in FIG. 9);

(2) converting the optical data signal to an electrical signal having a symbol rate (Specification p. 11, ln. 17 to p. 12, ln. 3; p. 13, lns. 16-28; p. 37, lns. 2-6; paras. [0065]-[0066] and [0073]; originally-filed claim 1; element 114 in FIGS. 1B-C and 11A; element 118 in FIG. 1C; and elements 904-1 to 904-4 in FIG. 9);

(3) generating N sampling signals having a first frequency that is lower than the symbol rate, the N sampling signals shifted in phase relative to one another, wherein N is an integer greater than one (Specification p. 11, lns. 4-12; p. 17, ln. 18 to p. 20, ln. 4; p. 22, lns. 12-24; p. 23, lns. 4-16; p. 24, lns. 14-20; p. 28, lns. 3-9; paras. [0063], [0108]-[0112], [0124], [0126]-[0127], [0132], and [0145]; element 1018 in FIGS. 10A-G and

12; element 1019 in FIGS. 10A-B, 10E-G, and 12; elements 1019-1 to 1019-N in FIGS. 10C-D and 10H; elements  $fs_{(1)}$  to  $fs_{(N)}$  in FIGS. 11B, 12, and 14-19; and element 1902 in FIG. 19);

(4) controlling N analog-to-digital converter ("ADC") paths with the N sampling signals to sample the electrical signal at the phases, to produce samples (Specification p. 19, ln. 17 to p. 20, ln. 4; p. 22, lns. 12-24; paras. [0111]-[0112] and [0124]; elements 1012-1 to 1012-N in FIGS. 10A-B and 14; element 1019 in FIGS. 10A-B and 12; and elements  $fs_{(1)}$  to  $fs_{(N)}$  in FIGS. 12, 14-17, and 19);

(5) performing at least one M-path parallel digital process on the samples, wherein M is greater than N (Specification p. 10, ln. 22 to p. 11, ln. 3; p. 12, lns. 4-11; p. 17, ln. 18 to p. 18, ln. 18; p. 19, lns. 17-26; p. 20, lns. 5-9; p. 20, lns. 14-27; p. 24, ln. 28 to p. 25, ln. 4; p. 28, ln. 25 to p. 30, ln. 8; p. 30, lns. 17-21; p. 37, lns. 2-6; paras. [0061]-[0062], [0067], [0108]-[0109], [0111], [0113], [0115]-[0116], [0134], [0150]-[0152], and [0155]; originally-filed claim 1; element 110 in FIGS. 10A-B; element 110-1 and elements labeled "DSP" in FIG. 9; elements 1014-1 to 1014-M in FIG. 10A; element 1016 in FIG. 10B; elements 1020 and 1022 in FIG. 10B; element 1208 in FIG. 12; element 1210 in FIGS. 12-13; element 1704 in FIG. 17; and the element labeled "feedforward equalizer" in FIGS. 15-17 and 19); and

(6) generating a digital signal representation of the optical data signal from the samples (Specification p. 43, lns. 4-30; p. 3, lns. 25-29; p. 10, lns. 14-17; p. 10, ln. 22 to p. 11, ln. 12; p. 11, ln. 17 to p. 12, ln. 17; p. 13, lns. 16-28; p. 16, ln. 27 to p. 17, ln. 2; p. 29, lns. 24-28; paras. [0012], [0059], [0061]-[0063], [0065]-[0068], [0073], [0104],

and [0151]; Abstract; elements 102 and 106 in FIGS. 1A-B, element 110 in FIGS. 1A-B, 10A-B, 12, and 17; element 110-1 and elements labeled "DSP" in FIG. 9; elements 1014-1 to 1014-M in FIG. 10A; and elements 1020 and 1022 in FIG. 10B).

Independent claim 9 recites an optical receiver. The optical receiver includes:

a receiver input (Specification p. 3, lns. 3-6; p. 10, ln. 14 to p. 13, ln. 28; p. 20, lns. 14-23; p. 20, ln. 28 to p. 21, ln. 22; p. 28, ln. 25 to p. 29, ln. 23; p. 30, lns. 12-16; p. 31, ln. 6 to p. 32, ln. 2; p. 38, lns. 2-7; paras. [0008], [0059]-[0073], [0115], [0117]-[0120], [0150], [0154], and [0158]-[0160]; originally-filed claim 9; element 102 in FIGS. 1A, 1C, 10B, 11B, 12, 14, and 17; element 112 in FIGS. 1A-B and 9; element 114 in FIGS. 1B-C and 11A; elements 903-1 to 903-4 in FIG. 9; element 1008 in FIGS. 10B, 12, 14, and 17; element 1108 in FIG. 11B; and elements 1402-1 to 1402N in FIG. 14);

an optical-to-electrical converter coupled to the receiver input (Specification p. 11, ln. 17 to p. 12, ln. 3; p. 13, lns. 16-28; paras. [0065]-[0066] and [0073]; element 114 in FIGS. 1B-C and 11A; element 118 in FIG. 1C; and elements 904-1 to 904-4 in FIG. 9);

an analog-to-digital converter ("ADC") array of N ADC paths, wherein N is an integer greater than 1, each ADC path including an ADC path input coupled to an output of the optical-to-electrical converter (Specification p. 3, ln. 7 to p. 3, ln. 11; p. 11, lns. 4-12; p. 13, lns. 16-28; p. 21, lns. 1-7; paras. [0009], [0063], [0073], and [0118]; and elements 108-1, 903-1 to 903-4, and 904-1 to 904-4 in FIG. 9); and

an M-path digital signal processor coupled to the ADC array, wherein M is greater than N (Specification p. 6, lns. 19-21; p. 10, lns. 22-26; p. 12, lns. 4-11; p. 13, lns. 16-28; p. 17, ln. 12 to p. 20, ln. 23; p. 21, lns. 1-7; p. 22, ln. 25 to p. 23, ln. 3; p. 23, ln. 17 to p. 24, ln. 4; paras. [0032], [0061]-[0064], [0067]-[0068], [0073], [0107]-[0115], [0118], [0125], and [0128]-[0130]; element 110 in FIGS. 1A-B, 10A-B, 12, and 17; element 110-1 and elements labeled "DSP" in FIG. 9; and elements 1014-1 to 1014-M in FIG. 10A).

Independent claim 18 recites an optical receiver. The optical receiver includes:

means for receiving an optical data signal (Specification p. 3, lns. 3-6; p. 11, ln. 17 to p. 13, ln. 28; p. 21, lns. 8-15; p. 39, lns. 1-6; paras. [0008], [0065]-[0073], and [0119]; originally-filed claim 18; element 102 in FIG. 1C; element 112 in FIGS. 1B and 9; element 114 in FIGS. 1B-C and 11A; and elements 903-1 to 903-4 in FIG. 9);

means for converting the optical data signal to an electrical signal having a symbol rate (Specification p. 11, ln. 17 to p. 12, ln. 3; p. 13, lns. 16-28; p. 39, lns. 1-6; paras. [0065]-[0066] and [0073]; originally-filed claim 18; element 114 in FIGS. 1B-C and 11A; element 118 in FIG. 1C; and elements 904-1 to 904-4 in FIG. 9);

means for generating N sampling signals having a first frequency that is lower than the symbol rate, the N sampling signals shifted in phase relative to one another (Specification p. 11, lns. 4-12; p. 17, ln. 18 to p. 20, ln. 4; p. 22, lns. 12-24; p. 23, lns. 4-16; p. 24, lns. 14-20; p. 28, lns. 3-9; paras. [0063], [0108]-[0112], [0124], [0126]-[0127], [0132], and [0145]; element 1018 in FIGS. 10A-G, 12, and 17; element 1019 in FIGS.

10A-B, 10E-G, and 12; elements 1019-1 to 1019-N in FIGS. 10C-D and 10H; element 1902 in FIG. 19; and elements  $fs_{(1)}$  to  $fs_{(N)}$  in FIGS. 11B, 12, 14-17, and 19);

means for controlling N analog-to-digital converter ("ADC") paths with the N sampling signals to sample the electrical signal at the phases to produce samples (Specification p. 19, ln. 17 to p. 20, ln. 4; p. 22, lns. 12-24; paras. [0111]-[0112] and [0124]; elements 1012-1 to 1012-N in FIGS. 10A-B and 14; element 1019 in FIGS. 10A-B and 12; and elements  $fs_{(1)}$  to  $fs_{(N)}$  in FIGS. 12, 14-17, and 19);

means for performing at least one M-path parallel digital process on the samples, wherein M is greater than N (Specification p. 10, ln. 22 to p. 11, ln. 3; p. 12, lns. 4-11; p. 17, ln. 18 to p. 18, ln. 18; p. 19, lns. 17-26; p. 20, lns. 5-9; p. 20, lns. 14-27; p. 24, ln. 28 to p. 25, ln. 4; p. 28, ln. 25 to p. 30, ln. 8; p. 30, lns. 17-21; p. 39, lns. 1-6; paras. [0061]-[0062], [0067], [0108]-[0109], [0111], [0113], [0115]-[0116], [0134], [0150]-[0152], and [0155]; originally-filed claim 18; element 110 in FIGS. 10A-B; element 110-1 and elements labeled "DSP" in FIG. 9; elements 1014-1 to 1014-M in FIG. 10A; element 1016 in FIG. 10B; elements 1020 and 1022 in FIG. 10B; element 1208 in FIG. 12; element 1210 in FIGS. 12-13; element 1704 in FIG. 17; and the element labeled "feedforward equalizer" in FIGS. 15-17 and 19); and

means for generating a digital signal representation of the optical data signal from the samples (Specification p. 43, lns. 4-30; p. 3, lns. 25-29; p. 10, lns. 14-17; p. 10, ln. 22 to p. 11, ln. 12; p. 11, ln. 17 to p. 12, ln. 17; p. 13, lns. 16-28; p. 16, ln. 27 to p. 17, ln. 2; p. 29, lns. 24-28; paras. [0012], [0059], [0061]-[0063], [0065]-[0068], [0073], [0104], and [0151]; Abstract; elements 102 and 106 in FIGS. 1A-B, element 110 in FIGS. 1A-B,

10A-B, 12, and 17; element 110-1 and elements labeled "DSP" in FIG. 9; elements 1014-1 to 1014-M in FIG. 10A; and elements 1020 and 1022 in FIG. 10B).



**VI. Grounds of Rejection to be Reviewed on Appeal (37 C.F.R. § 41.37(c)(1)(vi))**

A concise statement listing each ground of rejection presented for review follows.

**A. Ground 1**

Claims 1-42, 52, 54, and 56 were rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over European Patent Application Publication No. 1006697 to Azadet *et al.* (herein "Azadet") in view of *Electrical Signal Processing Techniques in Long-Haul, Fiber Optic Systems* (IEEE Transactions on Communications, Vol. 38, No. 9, September 1990, pp. 1439-1453) by Winters *et al.* (herein "Winters"), and further in view of U.S. Patent No. 6,842,458 to Reznic (herein "Reznic").

**B. Ground 2**

Claims 43-51 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Azadet in view of Winters and Reznic, and further in view of *Multicarrier Modulation for Data Transmission: An Idea Whose Time Has Come* (IEEE Communication Magazine, May 1990, pp. 5-14) by John A. Bingham (herein "Bingham").

**VII. Argument (37 C.F.R. § 41.37(c)(1)(vii))**

**A. Rejection of claims 1-42, 52, 54, and 56 under 35 U.S.C. § 103(a) over Azadet in view of Winters, and further in view of Reznic**

In the Final Office Action of April 9, 2008, claims 1-42, 52, 54, and 56 were rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Azadet in view of Winters, and further in view of Reznic.

**1. The Obviousness Rejection of Claims 1-42, 52, 54, and 56 is in Error and Must be Reversed**

**a) The Teachings of Azadet, Winters, and Reznic are Insufficient to Establish a Prima Facie Case of Obviousness because the Combination Fails to Teach, Suggest, or Disclose all Claimed Features**

Claims 1-42, 52, 54, and 56 are allowable because the combined teachings of Azadet, Winters, and Reznic fail to teach all claimed features of claims 1-42, 52, 54, and 56. In order to establish *prima facie* obviousness of a claimed invention using a combination of references, all claim limitations must be taught or suggested by the combination of cited references. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Further, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970); *see also* M.P.E.P. § 2143A.

For example, the features of independent claim 1 reciting, "controlling *N analog-to-digital converter* ("ADC") *paths* with the N sampling signals to sample the electrical signal at the phases, to produce samples; [and] performing at least one *M-path parallel digital process* on the samples, *wherein M is greater than N*" are features that distinguish claim 1 over Azadet, Winters, and Reznic. (emphasis added). Further, for example, the features of independent claim 9 reciting, "an analog-to-digital converter

("ADC") array of **N ADC paths**, wherein N is an integer greater than 1, each ADC path including an ADC path input coupled to an output of the optical-to-electrical converter; and an **M-path digital signal processor** coupled to the ADC array, **wherein M is greater than N**" are features that distinguish claim 9 over Azadet, Winters, and Reznic. (emphasis added). Also, for example, the features of independent claim 18 reciting, "means for controlling **N analog-to-digital converter ("ADC") paths** with the N sampling signals to sample the electrical signal at the phases to produce samples; means for performing at least one **M-path parallel digital process** on the samples, **wherein M is greater than N**" are features that distinguish claim 18 over Azadet, Winters, and Reznic. (emphasis added).

The Final Office Action, on pages 5, 7, and 10, repeatedly admits deficiencies of Azadet and Winters by stating "Azadet et al. in view of Winter [sic] et al. *do not* [sic] *expressly disclose wherein M is greater than N.*" (emphasis added). Reznic does not overcome these deficiencies of Azadet and Winters. Specifically, Reznic does not teach, suggest, or disclose a relationship between the number of ADC paths ("N") and the number of parallel digital process paths ("M") where  $M > N$ , as is recited in claims 1, 9, and 18. Instead, Reznic's FIG. 2 describes that two codecs 212 (i.e.  $N=2$ ) feed each respective DSP 214 (i.e.  $M=1$ ). Thus, in Reznic's FIG. 2, the number of digital paths (e.g. DSP 214, "M") is *less than* the number of ADCs (e.g. codecs 212, "N"), so Reznic discloses  $M < N$ , which does not teach, suggest, or disclose the Appellants' claimed invention having  $M > N$ .

Further, Reznic does not teach, suggest, or disclose  $M > N$  in column 2, lines 51-53 as asserted in the Response to Arguments on page 2 of the Final Office Action. The cited section of Reznic reads "[t]he outputs from **multiple ones of the codecs 212** are

processed by **one** of multiple digital signal processors ("DSPs") 214 included in the EU unit 200." *See*, Reznic, col. 2, lns. 51-53 (emphasis added). Thus, the statement in Reznic that "*multiple ones* of the codecs 212" describes "*N*" *greater than or equal to two* ( $N \geq 2$ ). *Id.* (emphasis added). The cited section then further states that the outputs "are processed by *one* of multiple digital signal processors", which describes "*M*" *equal to one*. ( $M=1$ ). *Id.* (emphasis added). With this statement, Reznic discloses  $M < N$ , which does not teach, suggest, or disclose the Appellants' claimed invention having  $M > N$ . Thus, Reznic does not overcome the deficiencies of Azadet in view of Winters. Again, this is clearly shown in FIG. 2, where **two** codecs 212 ("*N*") feed a **single** DSP 216 ("*M*"), so that  $N > M$  in Reznic. In marked contrast, the Appellants claim the opposite configuration, where  $M > N$ .

Further, in the Response to Arguments on page 2 of the Final Office Action, the Examiner cites to page 11, paragraph [0063], lines 5-6 of the Appellants' Specification as allegedly "clearly" teaching that Reznic teaches, suggests, or discloses that  $kN=M$ . The cited passage of the Appellants' Specification does not mention Reznic and thus does not support that Reznic teaches, suggests, or discloses that  $kN=M$ .

The proposed combination of Azadet, Winters, and Reznic does not teach each and every feature of independent claims 1, 9, and 18, and therefore does not meet the minimum requirements for establishing a *prima facie* case of obviousness. *See*, M.P.E.P. § 2143A. Accordingly, the proposed combination of Azadet, Winters, and Reznic also does not establish a *prima facie* case for respective dependent claims 2-8, 10-17, 19-42, 52, 54, and 56.

The arguments in the Final Office Action fail to overcome the Appellants' arguments presented in the previous Reply and fail to establish a *prima facie* case of obviousness of claims 1-42, 52, 54, and 56. Therefore, the Appellants respectfully request that the Board reverse the Examiner's final rejection of claims 1-42, 52, 54, and 56 under 35 U.S.C. § 103(a) and remand this application for issue.

**b) *Claims 1-42, 52, 54, and 56 are Non-Obvious Because Reznic Teaches Away from the Claims***

The Examiner also fails to establish a *prima facie* case of obviousness in the Final Office Action of claims 1-42, 52, 54, and 56 under 35 U.S.C. § 103(a) because Reznic teaches away from the claims. "A *prima facie* case of obviousness can be rebutted if the applicant . . . can show 'that the art in any material aspect taught away' from the claimed invention." *In re Geisler*, 116 F.3d 1465, 1469 (Fed. Cir. 1997). "A reference may be said to teach away when a person of ordinary skill, upon reading the reference . . . would be led in a direction divergent from the path that was taken by the applicant." *Tec Air, Inc. v. Denso Mfg. Mich. Inc.*, 192 F.3d 1353, 1360 (Fed. Cir. 1999). When determining if a cited reference teaches away, a reference should be considered as a whole, and portions arguing against or teaching away from the claimed invention must be considered. *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 796 F.2d 443, 230 USPQ 416 (Fed. Cir. 1986); *Gillette Co. v. S.C. Johnson & Sons, Inc.*, 919 F.2d 720, 724, 16 USPQ2d 1923, 1927 (Fed. Cir. 1990) (stating that the closest prior art reference "would likely discourage the art worker from attempting the substitution suggested by [the inventor/patentee]"). The United States Supreme Court has also opined about the impact of teaching away on nonobviousness, stating in *KSR Int'l. Co. v. Teleflex, Inc.* "[w]hen the prior art teaches away from combining certain known

elements, discovery of successful means of combining them is more likely to be nonobvious." 550 U.S. \_\_\_, 127 S. Ct. 1727, 82 U.S.P.Q.2d 1385 (2007).

Reznic teaches away from the above-identified distinguishing features of independent claims 1, 9, and 18. In particular, the Appellants' claims recite distinguishing features that are directed towards a relationship between the number of ADC paths ("N") and the number of parallel digital process paths ("M") where  $M > N$ .

In contrast, as explained above, Reznic explicitly teaches a relationship where  $M < N$ . Reznic, FIG. 2. Thus, since Reznic explicitly describes a relationship where  $M < N$ , Reznic leads the person of ordinary skill away from a relationship where  $M > N$ , down a divergent path from that claimed by the Appellants. A *prima facie* case of obviousness of independent claims 1, 9, and 18 is not established because Reznic explicitly teaches away from the claimed feature of a relationship where  $M > N$ . Accordingly, the proposed combination of Azadet, Winters, and Reznic also does not establish a *prima facie* case for respective dependent claims 2-8, 10-17, 19-42, 52, 54, and 56.

The arguments in the Final Office Action fail to overcome the Appellants' arguments presented in the previous Reply and fail to establish a *prima facie* case of obviousness of claims 1-42, 52, 54, and 56. Therefore, the Appellants respectfully request that the Board reverse the Examiner's Final Rejection of claims 1-42, 52, 54, and 56 under 35 U.S.C. § 103(a) and remand this application for issue.

**B.      *Rejection of Claims 43-51 under 35 U.S.C. § 103(a) over Azadet in view of Winters, Reznic, and Bingham***

In the Final Office Action of April 9, 2008, claims 43-51 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Azadet in view of Winters and Reznic, and further in view of Bingham.

**1.      *The Obviousness Rejection of Claims 43-51 is in Error and Must be Reversed***

**a)      *Claims 43-51 are Non-obvious by Being Dependent on Respective Non-Obvious Independent Claims***

Dependent claims 43-51 are allowable for being dependent from an allowable independent claim. In the case *In Re Fine*, six dependent claims depended from two non-obvious independent claims. 837 F.2d 1071, 1075 (Fed. Cir. 1988). The United States Court of Appeals for the Federal Circuit held that the six "[d]ependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." *Id.*; *see also*, M.P.E.P. § 2143.03.

As shown above, independent claims 1, 9, and 18 are non-obvious over Azadet in view of Winters, and further in view of Reznic. Just like the six dependent claims in the case *In Re Fine*, the Appellants' dependent claims 43-51 depend upon their respective non-obvious independent claims 1, 9, and 18, and are thus similarly allowable over the cited references for their dependency on an allowable base claim. *Id.* Further, the Final Office Action does not use Bingham to teach or suggest at least the distinguishing features discussed above with regard to independent claims 1, 9, and 18, nor does Bingham remedy the deficiencies of Azadet, Winters, and Reznic, either alone or in combination. Thus, dependent claims 43-51 are allowable for at least being dependent from an allowable independent claim, in addition to their own patentable features.

The arguments in the Final Office Action fail to overcome the Appellants' arguments presented in the previous Reply and fail to establish a *prima facie* case of obviousness of claims 43-51. Therefore, the Appellants respectfully request that the Board reverse the Examiner's final rejections of claims 43-51 under 35 U.S.C. § 103(a) and remand this application for issue.



**VIII. Conclusion**

The subject matter of claims 1-52, 54, and 56 is patentable over the cited references because the Examiner has failed to establish a *prima facie* case of obviousness. Therefore, the Appellants respectfully request that the Board reverse the Examiner's final rejections of claims 1-52, 54, and 56 under 35 U.S.C. § 103(a) and remand the '896 application for issue.

Respectfully submitted,

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***IX. Claims Appendix (37 C.F.R. § 41.37(c)(1)(viii))***

1. A method for receiving an optical data signal, comprising:
  - (1) receiving an optical data signal;
  - (2) converting the optical data signal to an electrical signal having a symbol rate;
  - (3) generating N sampling signals having a first frequency that is lower than the symbol rate, the N sampling signals shifted in phase relative to one another, wherein N is an integer greater than one;
  - (4) controlling N analog-to-digital converter ("ADC") paths with the N sampling signals to sample the electrical signal at the phases, to produce samples;
  - (5) performing at least one M-path parallel digital process on the samples, wherein M is greater than N; and
  - (6) generating a digital signal representation of the optical data signal from the samples.
2. The method according to claim 1, wherein step (5) further comprises performing an equalization process on the samples.
3. The method according to claim 2, wherein step (5) further comprises performing a Viterbi equalization process on the samples.
4. The method according to claim 2, wherein step (5) further comprises performing a feed-forward equalization process on the samples.

5. The method according to claim 2, wherein step (5) further comprises performing a decision feedback equalization process on the samples.
6. The method according to claim 2, wherein step (5) further comprises performing Viterbi equalization and feed-forward equalization processes on the samples.
7. The method according to claim 2, wherein step (5) further comprises performing Viterbi equalization and decision feedback equalization processes on the samples.
8. The method according to claim 2, wherein step (5) further comprises:  
performing one or more of the following types of equalization processes on the samples:
  - Viterbi equalization;
  - feed-forward equalization; and
  - decision feedback equalization.
9. An optical receiver, comprising:
  - a receiver input;
  - an optical-to-electrical converter coupled to the receiver input;
  - an analog-to-digital converter ("ADC") array of N ADC paths, wherein N is an integer greater than 1, each ADC path including an ADC path input coupled to an output of the optical-to-electrical converter; and
  - an M-path digital signal processor coupled to the ADC array, wherein M is greater than N.

10. The optical receiver according to claim 9, wherein the digital signal processor includes an equalizer.
11. The optical receiver according to claim 10, wherein the equalizer comprises a Viterbi equalizer.
12. The optical receiver according to claim 10, wherein the equalizer comprises a feed-forward equalizer.
13. The optical receiver according to claim 10, wherein the equalizer comprises a decision feedback equalizer.
14. The optical receiver according to claim 10, wherein the equalizer comprises a Viterbi equalizer and a feed-forward equalizer.
15. The optical receiver according to claim 10, wherein the equalizer comprises a Viterbi equalizer and a decision feedback equalizer.
16. The optical receiver according to claim 10, wherein the equalizer comprises a feed-forward equalizer and a decision feedback equalizer.
17. The optical receiver according to claim 10 wherein the equalizer comprises one or more of:
  - a Viterbi equalizer;
  - a feed-forward equalizer; and

a decision feedback equalizer.

18. An optical receiver, comprising:

means for receiving an optical data signal;

means for converting the optical data signal to an electrical signal having a symbol rate;

means for generating N sampling signals having a first frequency that is lower than the symbol rate, the N sampling signals shifted in phase relative to one another;

means for controlling N analog-to-digital converter ("ADC") paths with the N sampling signals to sample the electrical signal at the phases to produce samples;

means for performing at least one M-path parallel digital process on the samples, wherein M is greater than N; and

means for generating a digital signal representation of the optical data signal from the samples.

19. The system according to claim 18, wherein the means for performing digital processes on the samples include means for equalizing the samples.

20. The system according to claim 19, wherein the means for equalizing the samples comprise means for performing a Viterbi equalization process on the samples.

21. The system according to claim 19, wherein the means for equalizing the samples comprise means for performing a feed-forward equalization process on the samples.

22. The system according to claim 19, wherein the means for equalizing the samples comprise means for performing a decision feedback equalization process on the samples.

23. The system according to claim 19, wherein the means for equalizing the samples comprise means for performing Viterbi equalization and feed-forward equalization processes on the samples.

24. The system according to claim 19, wherein the means for equalizing the samples comprises means for performing Viterbi equalization and decision feedback equalization processes on the samples.

25. The method according to claim 2, wherein step (1) comprises receiving the optical data signal from a multimode optical fiber and step (5) comprises equalizing multimode dispersion from the multimode optical fiber.

26. The method according to claim 2, wherein step (1) comprises receiving the optical data signal from a single mode optical fiber and step (5) comprises equalizing chromatic and/or waveguide dispersion from the single mode optical fiber.

27. The method according to claim 2, wherein step (1) comprises receiving the optical data signal from a multimode optical fiber and step (5) comprises equalizing chromatic and/or waveguide dispersion from the multimode optical fiber.

28. The method according to claim 2, wherein step (1) comprises receiving the optical data signal from a single mode optical fiber and step (5) comprises equalizing polarization mode dispersion from the single mode optical fiber.

29. The method according to claim 2, wherein step (1) comprises receiving the optical data signal from a single mode optical fiber and step (5) comprises equalizing dispersion induced in the single mode optical fiber by laser chirping.

30. The method according to claim 2, wherein step (1) comprises receiving the optical data signal from a transmitter that lacks external modulators, and step (5) comprises equalizing excess dispersion induced by laser chirping.

31. The optical receiver according to claim 10, wherein the input is coupled to a multimode optical fiber and the equalizer equalizes multimode dispersion from the multimode optical fiber.

32. The optical receiver according to claim 10, wherein the input is coupled to a single mode optical fiber and the equalizer equalizes chromatic and/or waveguide dispersion from the single mode optical fiber.

33. The optical receiver according to claim 10, wherein the input is coupled to a multimode optical fiber and the equalizer equalizes chromatic and/or waveguide dispersion in the multimode optical fiber.

34. The optical receiver according to claim 10, wherein the input is coupled to a multimode optical fiber and the equalizer equalizes polarization mode dispersion from the single mode optical fiber.

35. The optical receiver according to claim 10, wherein the input is coupled to a single mode optical fiber and the equalizer equalizes dispersion induced in the single mode optical fiber by laser chirping.

36. The optical receiver according to claim 10, wherein the input receives the optical data signal from a transmitter that lacks external modulators, and the equalizer equalizes excess dispersion induced by laser chirping.

37. The optical receiver according to claim 19, wherein the means for receiving an optical signal is coupled to a multimode optical fiber and the means for equalizing comprises means for equalizing multimode dispersion from the multimode optical fiber.

38. The optical receiver according to claim 19, wherein the means for receiving an optical signal is coupled to a single mode optical fiber and the means for equalizing comprises means for equalizing chromatic and/or waveguide dispersion from the single mode optical fiber.

39. The optical receiver according to claim 19, wherein the means for receiving an optical signal is coupled to a multimode optical fiber and the means for equalizing comprises means for equalizing chromatic and/or waveguide dispersion in the multimode optical fiber.



40. The optical receiver according to claim 19, wherein the means for receiving an optical signal is coupled to a multimode optical fiber and the means for equalizing comprises means for equalizing polarization mode dispersion from the single mode optical fiber.

41. The optical receiver according to claim 19, wherein the means for receiving an optical signal is coupled to a single mode optical fiber and the means for equalizing comprises means for equalizing dispersion induced in the single mode optical fiber by laser chirping.

42. The optical receiver according to claim 19, wherein the means for receiving an optical signal receives the optical data signal from a transmitter that lacks external modulators, and the means for equalizing comprises means for equalizing excess dispersion induced by laser chirping.

43. The method according to claim 1, wherein step (5) comprises decoding a convolutional code.

44. The method according to claim 1, wherein step (5) comprises decoding a trellis code.

45. The method according to claim 1, wherein step (5) comprises decoding a block code.

46. The optical receiver according to claim 9, wherein the digital signal processor comprises a convolutional decoder.
47. The optical receiver according to claim 9, wherein the digital signal processor comprises a trellis decoder.
48. The optical receiver according to claim 9, wherein the digital signal processor comprises a block decoder.
49. The optical receiver according to claim 18, wherein the means for performing digital processes on the samples comprises means for decoding a convolutional code.
50. The optical receiver according to claim 18, wherein the means for performing digital processes on the samples comprises means for decoding a trellis code.
51. The optical receiver according to claim 18, wherein the means for digitally performing digital processes on the samples comprises means for decoding a block code.
52. The method according to claim 1, wherein  $M$  equals  $2N$ .
54. The optical receiver according to claim 9, wherein  $M$  equals  $2N$ .
56. The system according to claim 18, wherein  $M$  equals  $2N$ .

***X. Evidence Appendix (37 C.F.R. § 41.37(c)(1)(ix))***

None.

***XI. Related Proceedings Appendix (37 C.F.R. § 41.37(c)(1)(x))***

None.